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Fig. 1

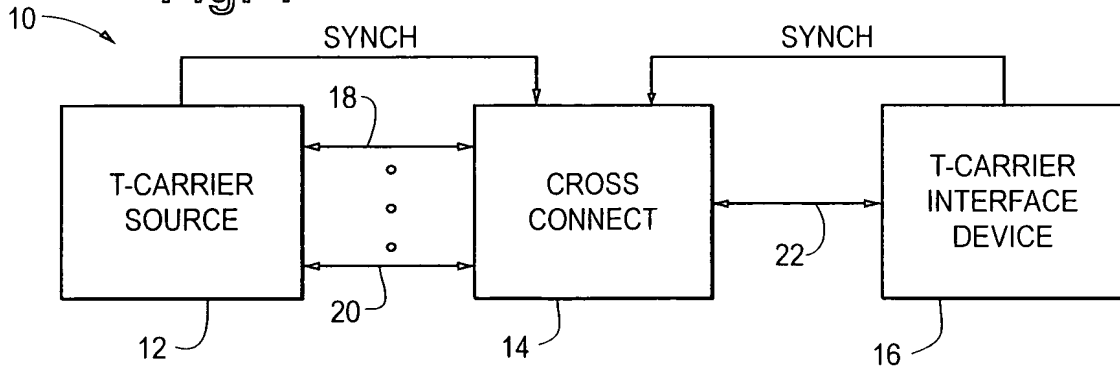


Fig. 2

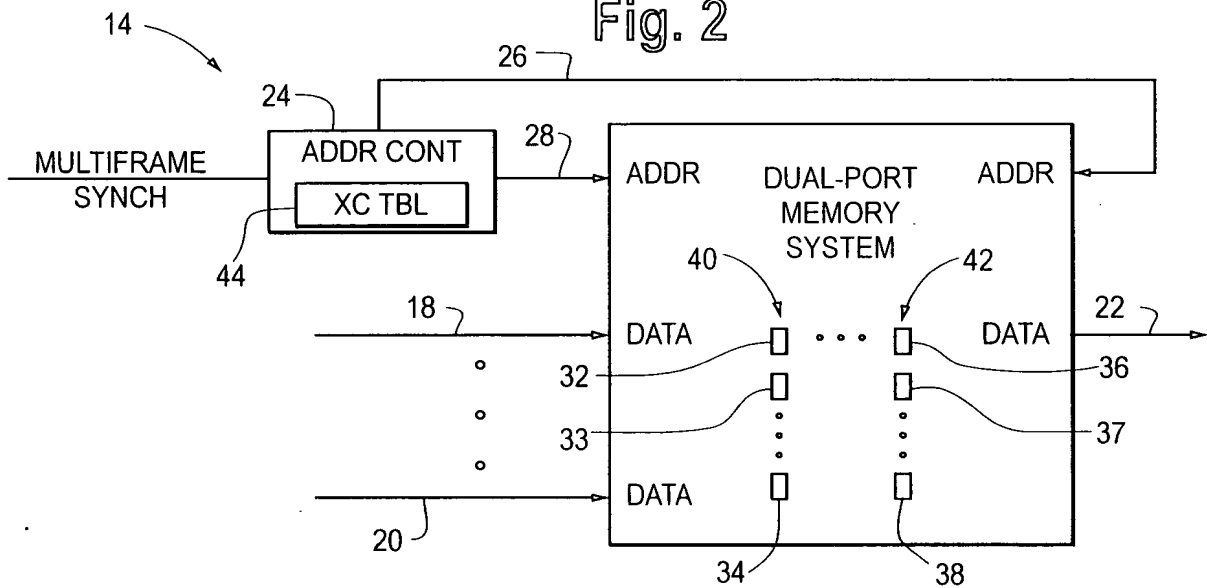


Fig. 3

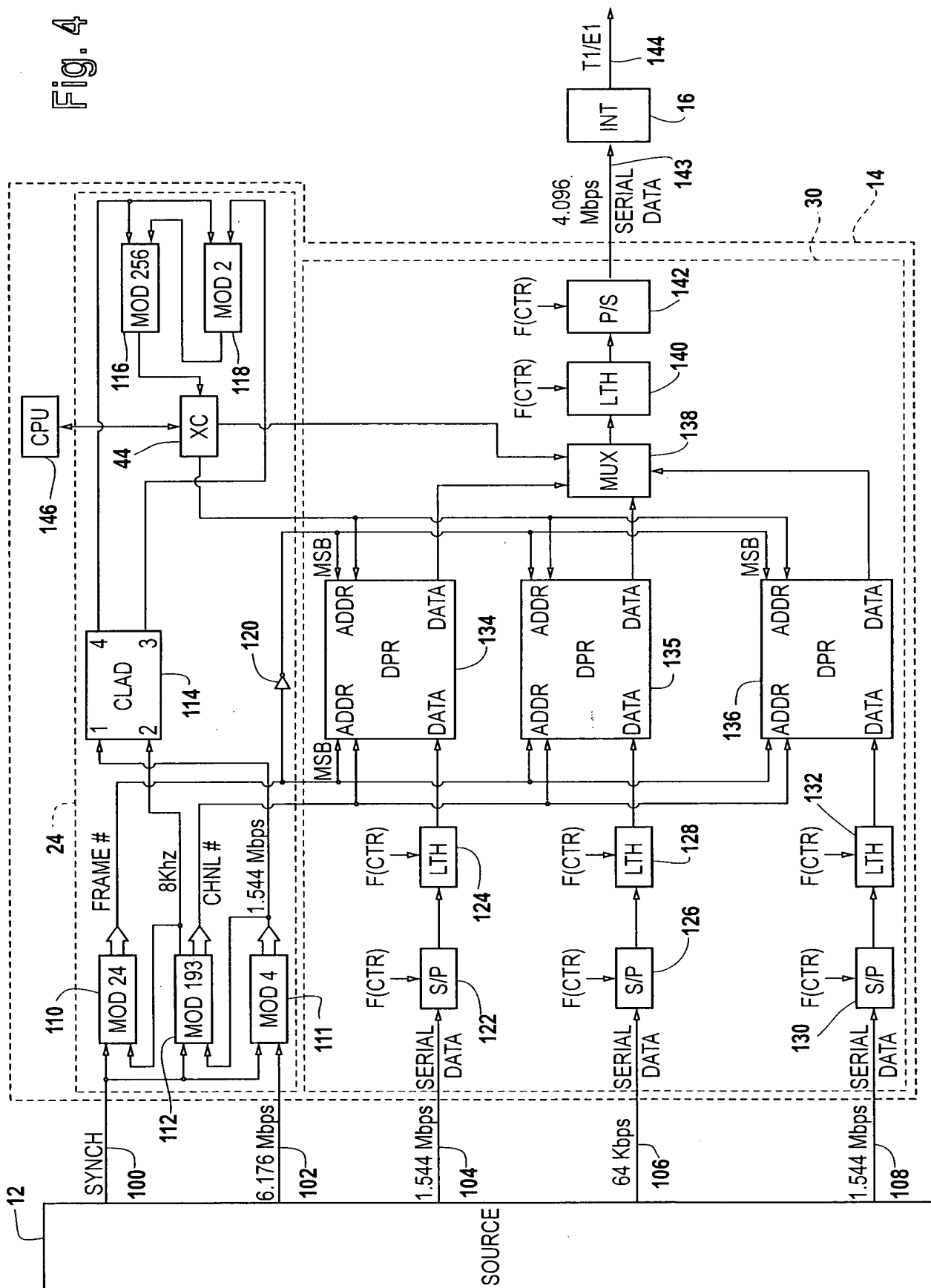
Fig. 3 is a table 44 showing a mapping of input/output channels to memory addresses. The table has three columns: an unlabeled column, column 46, column 48, and column 50. The rows are numbered 1 through 24.

	46	48	50
1	40	20	
2	40	7	
3	42	1	
4	40	3	
...			
21	42	3	
22	42	18	
23	-	-	
24	-	-	



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Fig. 4



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Fig. 5

